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# Reactive Ion Etching of PECVD Silicon Dioxide ($SiO_2$) Layer for MEMS Application

by Derwin Washington

ARL-TR-3269 July 2004

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**Sensors and Electron Devices Directorate, ARL**

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A reactive ion etching (RIE) process has been developed to etch up to 1-micrometer (1 μm) layer of low stress $SiO_2$ (Silicon Dioxide) Plasma Enhanced Chemical Vapor Deposition (PECVD) film compatible for MEMS research applications. Etch rates from as low as 123 nm/min at 100 W to as high as 721 nm/min at 900 W powers were demonstrated using fluorocarbon ($CF_4$) reactive gas plasma. RIE selectivity ($SiO_2$/PR-Photoresist was 3:1 at 900W. The measured thickness variation was 0.13 μm on 4-inch substrate for 1 μm thick $SiO_2$ film.

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# 1. Introduction

One of the most important elements of dry etching $SiO_2$ film patterns is that critical feature dimensions should not alter during the etching period, a parameter that must be maintained for optimum operation and reproducibility of the MEMS device. This means that the photo resist mask pattern used for pattern transfer must also maintain its dimensions and have a much lower etch rate than the $SiO_2$ film it is etching.

## 1.1 Wet and Dry Etching

For advanced device fabrication, RIE is advantageous for precise pattern transfer that is not achievable using conventional wet etching. RIE is an anisotropic method that faithfully reproduces the mask pattern features as shown in figure 1. Conventional wet chemical etching is isotropic in nature and causes undercutting of the $SiO_2$ material beneath the mask pattern due to substantial different etch rate at the interfaces. Wet chemical etching is an isotropic process and will create $SiO_2$ film features that are always different than the photo resist mask pattern as shown in figure 2. One of the main problems in the wet chemical etching is the complete neutralization of trace amount of wet chemical in-between the interfaces. Chemical reaction can continue even long after removal from the etching solutions, and treating with an appropriate neutralizer and water. Such post etching will create disastrous results in due process.

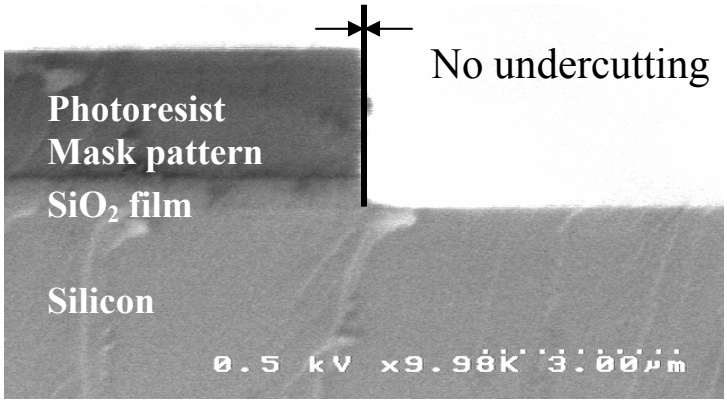


Figure 1. Scanning Electron Microscope image cross-section of a $SiO_2$ film after RIE.

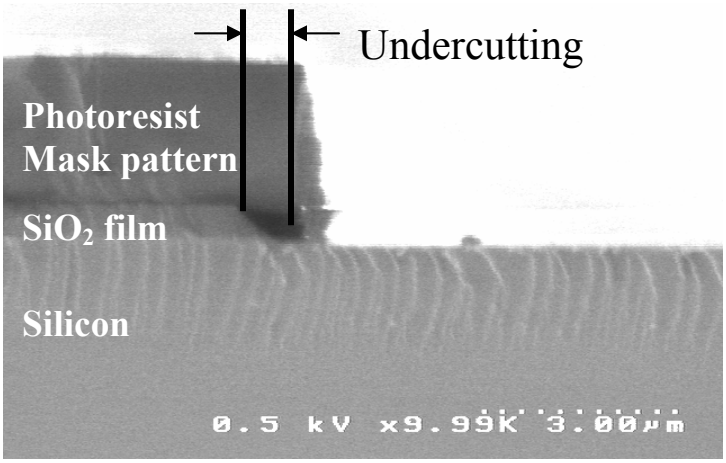


Figure 2. Scanning Electron Microscope image cross-section of a $SiO_2$ film after wet etching.

### 1.2 PECVD $SiO_2$ Deposition

PECVD method has many advantages over conventional Low Pressure Chemical Vapor Deposition (LPCVD) method. In today's very large-scale integrated circuit, $SiO_2$ is mainly used as a conformal passivation layer over topographical surface features. In MEMS device applications the $SiO_2$ film is additionally being used for mechanical support structure of a beam structure. PECVD$SiO_2$ films have the advantage of being deposited at relatively low temperatures (250-300ºC) compared to conventional LPCVD (400-450ºC), and steam grown silicon dioxide (900-950ºC). High temperatures can cause detrimental affects to previously deposited materials and must be avoided. Even at low deposition temperature the residual stress of PECVD films is affected by the stoichiometry and can cause bowing of fabricated beams or freestanding structures in MEMS devices if not controlled. Another advantage of PECVD films is the chemical stoichiometry can be controlled to a great degree in order to minimize the residual stress of the deposited films. We previously studied stress reduction methods in MEMS structures consisting of PECVD deposited $SiO_2$ films (*1*), for piezoelectric PZT sensor and actuator devices (*2,3*).

### 1.3 RIE of Silicon Dioxide

Commercial automated RIE system Lam 590 was used in this experiment. The plasma etcher system is equipped with cassette-to-cassette loading, and can operate at low pressure, low bias, high-density, between 0 to 1250-Watts. The etcher uses a mixture of gases $CF_4$, $CHF_3$, and He to anisotropically etch dielectric thin films. The etcher has two sub-chambers (load-locks) to prevent contamination and particulates of the main chamber during loading and unloading of the wafers. It has a built-in optical end-point detection systems, with the option of performing an over-etch either through a set time or by a percentage of the main etch. The chuck used for holding the wafer was water-cooled and the spacing gap between the wafer and top electrode was variable.

## 2. Experiment

The 1 μm thick $SiO_2$ films were first deposited on 4-inch diameter <100> silicon wafer using Unaxis PECVD system model 790 at 250ºC temperature. The dielectric films were annealed using a Heatpulse 610 rapid thermal annealer (RTA) at 700ºC with $N_2$ flowing at 1 atmosphere for 60 seconds to densify and remove trapped hydrogen byproducts. The film thickesses were measured non-destructively using a J.A. Woollam M-2000 ellipsometer. The variables parameters for this etch experiments were etch time and power. All the $SiO_2$ films were mask patterned with test structures, and finally RIE at 30 second intervals until all the $SiO_2$ was removed. I prepared the mask pattern by the photo resist lithography (appendix A) method and its thickness was measured using a Tenor Model P-15 profilometer. The first 5 samples were prepared with blanket $SiO_2$, and 19 other samples mask patterned with AZ 5214E photo resist on top the $SiO_2$ film. The photo resist test mask patterns consisted of lines and spaces with the following dimensions: 2, 5, 10, 20, 50, 100, 500, and 1000 um. The object of this experiment was to transfer the photo resist mask pattern into the $SiO_2$ film using RIE. The etching parameters for this experiment are listed in appendix B. A picture of the Lam 590 reactor used in this experiment is shown in figure 3.

Figure 3. Picture of Lam 590 Auto System for etching $SiO_2$ films.

## 3. Discussion and Results

The data shown in table 1 are for 5 wafers with blanket $SiO_2$ films and the measurements were taken from four different locations on the wafer before and after each 30-second etch interval to determine uniformity of the etch. I used a relatively high power setting 800 W and etched repeatedly until the $SiO_2$ film was completely removed. The average etch rate was calculated by measuring the film thickness at four positions divided by time in seconds. The average etch rate was 20.5 nm/sec based on 30-sec. etch interval. The film was completely removed after 120 seconds. The calculated etch rate based on 120-sec. interval was very low for all films in table 1 and is not the real etch rate. Just as an example, consider the etch rate of wafer #1 to be 20.5 nm at the 30 sec. Interval. The projected time to completely remove the starting film thickness is 45 sec. (20.5 nm/s x 927 nm). The remaining 75 sec. of the 120 sec. etch time contributes nothing to the actual etching and this is the reason for the low calculated etch rates. For this reason in the next experiment the etch time will be controlled more strictly to 30 sec. intervals in order to measure the etch rate more accurately when the film actually clears. The maximum observed variation in films etched across the entire 4-inch diameter wafer (substrate) was a low 39.9 nm for a 1 μm thick film.

Table 1. $SiO_2$film thickness as a function of etch time (800 W) without a P.R. mask pattern.

| Wafer # | Time (s) | Right (nm) | Center (nm) | Left (nm) | Top (nm) | Avg (nm) | Std Dev (nm) | Etch Rate (nm/s) |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| 0 | 0 | 928 | 928 | 927 | 924 | 926 | 1.7 | 0.0 |
| | 30 | 331 | 332 | 291 | 299 | 313 | 21.2 | 20.5 |
| | 120 | 0 | 0 | 0 | 0 | 0 | 0.0 | 7.7 |
| 1 | 0 | 986 | 980 | 986 | 957 | 977 | 13.9 | 0.0 |
| | 30 | 324 | 388 | 338 | 292 | 336 | 39.9 | 21.4 |
| | 120 | 0 | 0 | 0 | 0 | 0 | 0.0 | 8.1 |
| 2 | 0 | 981 | 974 | 971 | 985 | 978 | 6.1 | 0.0 |
| | 30 | 345 | 393 | 348 | 338 | 356 | 25.2 | 20.7 |
| | 120 | 0 | 0 | 0 | 0 | 0 | 0.0 | 8.1 |
| 3 | 0 | 983 | 985 | 997 | 1000 | 991 | 8.3 | 0.0 |
| | 30 | 344 | 401 | 346 | 373 | 366 | 26.4 | 20.8 |
| | 120 | 0 | 0 | 0 | 0 | 0 | 0.0 | 8.3 |
| 4 | 0 | 974 | 985 | 993 | 988 | 985 | 8.0 | 0.0 |
| | 30 | 360 | 396 | 381 | 361 | 374 | 17.4 | 20.4 |
| | 120 | 0 | 0 | 0 | 0 | 0 | 0.0 | 8.2 |
| | | | | | | | | Avg=20.76 |

The data shown in table 2 is for 5 silicon wafers patterned with photo resist over the $SiO_2$ films. The average etch rate is 12.05 nm/sec for 900 W power and is much lower (20.76 nm/sec) than what was observed previously for 800 W. A so-called loading effect occurs as the result of gas phase etchants species being depleted by reaction with the $SiO_2$ material (*4*). The number of

radicals in the plasma is in proportion to the number of atoms to be removed. In this case the patterned mask reduced the area of exposed $SiO_2$ and caused the slower reaction and therefore a slower etch rate. The maximum observed variation for wafers #'s 5-9 across the 4-inch diameter is a low 22.2 nm for a 1 μm thick film.

Table 2. $SiO_2$ film thickness as a function of etch time (900 W) with a P.R. mask pattern.

| Wafer # | Time (s) | Right (nm) | Center (nm) | Left (nm) | Top (nm) | Avg (nm) | Std Dev (nm) | Etch Rate (nm/s) |
|---|---|---|---|---|---|---|---|---|
| 5 | 0 | 1124 | 1125 | 1123 | 1114 | 1122 | 4.9 | 0.0 |
| | 30 | 777 | 759 | 779 | 772 | 772 | 8.9 | 11.7 |
| | 60 | 404 | 374 | 410 | 413 | 400 | 17.6 | 12.0 |
| | 90 | 0 | 26 | 35 | 42 | 26 | 18.3 | 12.2 |
| 6 | 0 | 1142 | 1131 | 1144 | 1127 | 1136 | 8.4 | 0.0 |
| | 30 | 768 | 755 | 778 | 761 | 766 | 9.9 | 12.4 |
| | 60 | 377 | 389 | 420 | 414 | 400 | 20.4 | 12.3 |
| | 90 | 13 | 0 | 31 | 47 | 23 | 20.7 | 12.4 |
| 7 | 0 | 1086 | 1083 | 1094 | 1091 | 1088 | 5.3 | 0.0 |
| | 30 | 717 | 706 | 726 | 736 | 721 | 12.7 | 12.2 |
| | 60 | 342 | 315 | 350 | 368 | 344 | 22.2 | 12.4 |
| | 90 | 0 | 0 | 0 | 0 | 0 | 0.0 | 12.1 |
| 8 | 0 | 1106 | 1099 | 1081 | 1088 | 1093 | 11.1 | 0.0 |
| | 30 | 749 | 741 | 744 | 738 | 743 | 4.7 | 11.7 |
| | 60 | 388 | 368 | 383 | 384 | 381 | 8.9 | 11.9 |
| | 90 | 26 | 0 | 33 | 24 | 21 | 14.2 | 11.9 |
| 9 | 0 | 1067 | 1070 | 1067 | 1060 | 1066 | 4.4 | 0.0 |
| | 30 | 699 | 697 | 716 | 705 | 704 | 8.7 | 12.0 |
| | 60 | 343 | 327 | 376 | 361 | 352 | 21.3 | 11.9 |
| | 90 | 0 | 0 | 0 | 0 | 0 | 0.0 | 11.8 |
| | | | | | | | | Avg=12.05 |

A study of the reliability of the photoresist mask against the reactive plasma gas chemistry was performed. In principal the mask must have a much lower etch rate in comparison to the $SiO_2$ material being etched. I used 9 wafers prepared with $SiO_2$ film and patterned with photo resist and etched at 30 sec intervals for a total of 90 sec. The etch rate to remove all $SiO_2$ film was previously demonstrated in table 2. To quantify the etch rate of the photo resist pattern, it was initially deposited over a bare silicon wafer instead of over $SiO_2$ film. If a layer of $SiO_2$ was used, it would have etched together with the photoresist and calculating the etch rate of two films at the same time would have required additional measurements. To make sure the silicon wafer did not react with the etchants, the photoresist was removed after completion of the etch experiment, and the surface profile was measured using a profiler. The surface showed latent images of the patterned photoresist, but the measured step height was negligible, indicating no etching of the silicon material actually occurred. The calculated etch rate of the photo resist is 4.1 nm/sec, and is the sum of all the etch rate data in table 3 divided by the number of data. At this rate, a starting photoresist pattern thickness of 1700 nm will last approximately 415 sec, at

least 4.6 times the amount of time needed to completely etch a 1 um thick $SiO_2$ film. This is a good safety margin for MEMS patterning application. A more common term used for measuring etch resistance is called "selectivity." Selectivity is defined as the etch rate ratio of $SiO_2$: photo resist; in this case 3:1 for 900 W power-setting conditions. The maximum observed deviation across the 4-inch diameter during any of the etching conditions was a low value of 42.3 nm.

Table 3. Patterned photo resist thickness on silicon substrate as function of etch time (900 W).

| Wafer # | Time (s) | Right (nm) | Top (nm) | Left (nm) | Bottom (nm) | Avg (nm) | Std Dev (nm) | Etch Rate (nm/s) |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1725 | 1716 | 1724 | 1706 | 1718 | 8.8 | 0.0 |
| | 30 | 1565 | 1558 | 1576 | 1555 | 1563 | 9.3 | 5.1 |
| | 60 | 1418 | 1399 | 1423 | 1403 | 1411 | 11.6 | 5.1 |
| | 90 | 1260 | 1244 | 1271 | 1254 | 1257 | 11.5 | 5.1 |
| 2 | 0 | 1854 | 1845 | 1824 | 1817 | 1835 | 17.2 | 0.0 |
| | 30 | 1683 | 1670 | 1650 | 1654 | 1664 | 15.3 | 5.7 |
| | 60 | 1532 | 1512 | 1494 | 1499 | 1509 | 16.8 | 5.4 |
| | 90 | 1236 | 1256 | 1226 | 1236 | 1239 | 12.8 | 6.6 |
| 3 | 0 | 1707 | 1693 | 1709 | 1716 | 1706 | 9.5 | 0.0 |
| | 30 | 1543 | 1533 | 1553 | 1552 | 1545 | 9.0 | 5.4 |
| | 60 | 1401 | 1372 | 1386 | 1402 | 1390 | 14.3 | 5.3 |
| | 90 | 1248 | 1214 | 1231 | 1247 | 1235 | 16.1 | 5.2 |
| 4 | 0 | 1702 | 1696 | 1712 | 1703 | 1703 | 6.9 | 0.0 |
| | 30 | 1547 | 1537 | 1540 | 1550 | 1543 | 5.9 | 5.4 |
| | 60 | 1404 | 1406 | 1402 | 1395 | 1402 | 5.0 | 5.1 |
| | 90 | 1254 | 1236 | 1244 | 1252 | 1246 | 8.4 | 5.1 |
| 5 | 0 | 1637 | 1654 | 1658 | 1663 | 1653 | 11.4 | 0.0 |
| | 30 | 1471 | 1482 | 1493 | 1495 | 1485 | 11.0 | 5.6 |
| | 60 | 1325 | 1335 | 1349 | 1344 | 1338 | 10.7 | 5.2 |
| | 90 | 1197 | 1194 | 1200 | 1164 | 1189 | 16.9 | 5.2 |
| 6 | 0 | 1883 | 1870 | 1853 | 1867 | 1868 | 12.4 | 0.0 |
| | 30 | 1855 | 1843 | 1820 | 1824 | 1835 | 16.4 | 1.1 |
| | 60 | 1852 | 1841 | 1849 | 1825 | 1842 | 12.4 | 0.4 |
| | 90 | 1848 | 1839 | 1832 | 1823 | 1835 | 10.8 | 0.4 |
| 7 | 0 | 1866 | 1877 | 1856 | 1871 | 1868 | 8.7 | 0.0 |
| | 30 | 1803 | 1812 | 1788 | 1722 | 1781 | 40.9 | 2.9 |
| | 60 | 1746 | 1755 | 1719 | 1663 | 1721 | 41.6 | 2.4 |
| | 90 | 1665 | 1697 | 1687 | 1603 | 1663 | 42.3 | 2.3 |
| 8 | 0 | 1865 | 1878 | 1889 | 1869 | 1875 | 10.9 | 0.0 |
| | 30 | 1778 | 1782 | 1803 | 1777 | 1785 | 12.4 | 3.0 |
| | 60 | 1698 | 1704 | 1719 | 1698 | 1705 | 10.1 | 2.8 |
| | 90 | 1612 | 1619 | 1638 | 1613 | 1620 | 12.2 | 2.8 |
| 9 | 0 | 1896 | 1901 | 1866 | 1864 | 1882 | 19.4 | 0.0 |
| | 30 | 1772 | 1776 | 1745 | 1744 | 1759 | 16.7 | 4.1 |
| | 60 | 1629 | 1660 | 1644 | 1632 | 1641 | 14.2 | 4.0 |
| | 90 | 1505 | 1531 | 1534 | 1510 | 1520 | 14.7 | 4.0 |
| | | | | | | | | Avg=4.1 |

During the fabrication of MEMS devices, sometimes there is a need to etch different thickness of $SiO_2$ layers. Other requirements include changing the power settings in order to improve the etch selectivity of adjoining structures or to minimize ion induced damage in parts of the device. It is important to have etch rate data for several power settings to accommodate the different fabrication process requirements. In table 4, the average etch rate is shown to increase with power. At 100 W the $SiO_2$ etch rate is not constant enough to predict film etching based on timing. On the other hand, this low power setting can be advantageous for removing thin film residues with extended time limits without effecting or etching other parts of the MEMS structures. The RIE process completely etched the $SiO_2$ films. The maximum observed variation across the entire 4-inch diameter wafer was no more than 13.3 nm for a 1 μm thick film.

Table 4. Etch rate of $SiO_2$ as a function of power with a P.R. mask pattern.

| Wafer # | Power (W) | Time (s) | Right (nm) | Center (nm) | Left (nm) | Top (nm) | Avg. (nm) | Std. Dev. (nm) | Etch Rate (nm/s) |
|---|---|---|---|---|---|---|---|---|---|
| 10 | 100 | 0 | 1100 | 1097 | 1082 | 1072 | 1088 | 13.3 | 0.0 |
| | | 30 | 1039 | 1035 | 1012 | 1019 | 1026 | 12.5 | 2.1 |
| | | 60 | 1039 | 1035 | 1012 | 1019 | 1026 | 12.8 | 1.0 |
| | | 90 | 1039 | 1037 | 1013 | 1019 | 1027 | 13.1 | 0.7 |
| | | 120 | 1039 | 1034 | 1013 | 1019 | 1026 | 12.4 | 0.5 |
| 11 | 300 | 0 | 1090 | 1083 | 1076 | 1075 | 1081 | 7.0 | 0.0 |
| | | 30 | 964 | 961 | 944 | 954 | 956 | 8.7 | 4.2 |
| | | 60 | 843 | 840 | 821 | 837 | 835 | 9.6 | 4.1 |
| | | 90 | 716 | 713 | 695 | 714 | 709 | 9.8 | 4.1 |
| 12 | 500 | 0 | 1095 | 1102 | 1088 | 1075 | 1090 | 11.5 | 0.0 |
| | | 30 | 912 | 913 | 904 | 895 | 906 | 8.3 | 6.1 |
| | | 60 | 733 | 724 | 722 | 713 | 723 | 8.0 | 6.1 |
| | | 90 | 547 | 541 | 537 | 533 | 539 | 5.7 | 6.1 |
| 13 | 700 | 0 | 1086 | 1092 | 1072 | 1077 | 1082 | 9.0 | 0.0 |
| | | 30 | 840 | 835 | 826 | 837 | 835 | 6.1 | 8.2 |
| | | 60 | 581 | 567 | 570 | 587 | 576 | 9.3 | 8.4 |
| | | 90 | 321 | 298 | 312 | 329 | 315 | 13.0 | 8.5 |
| 14 | 900W | 0 | 1085 | 1086 | 1083 | 1084 | 1085 | 1.5 | 0.0 |
| | | 30 | 725 | 726 | 723 | 724 | 725 | 1.5 | 12.0 |
| | | 60 | 365 | 366 | 363 | 364 | 365 | 1.5 | 12.0 |
| | | 90 | 5 | 6 | 3 | 4 | 5 | 1.5 | 12.0 |

A plot of the average etch rate for $SiO_2$ film as a function of power is shown in figure 4. The etch response is almost linear with time. Using this chart one can reliably project the time needed to etch any PECVD $SiO_2$ film up to 1 μm thickness range using this Lam 590 RIE system.

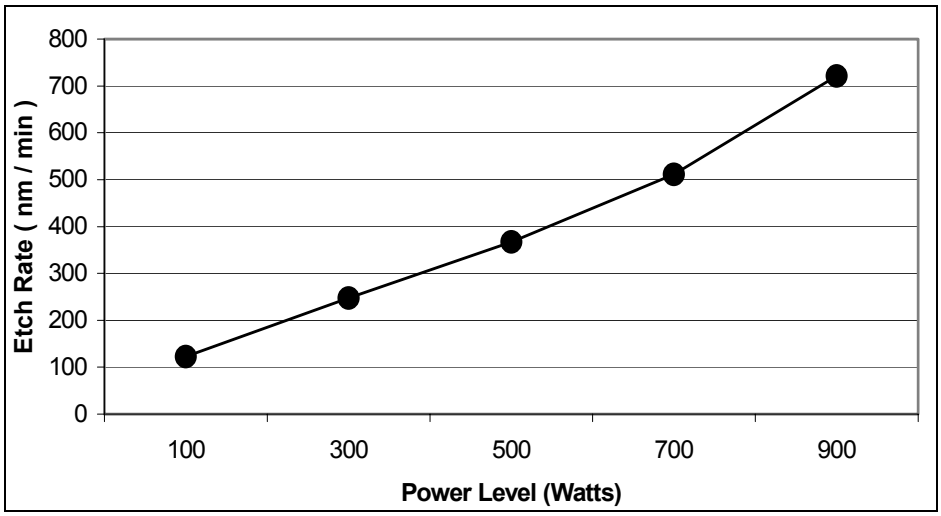


Figure 4. Plot of the average etch rate for $SiO_2$ film as a function of power.

In one specific application, we demonstrated anisotropic etch of a $SiO_2$ layer for a PZT MEMS resonator; picture shown in figure 5. The operational frequency of this resonator filter for communication is directly influenced by the material properties, as well as the dimensional tolerances of the beam structure. The dry etched $SiO_2$ film maintained a vertical profile similar the PZT piezoelectric material above it. The final resonator device operated very close to its predicted mechanical behavior due to the precise control of the $SiO_2$ critical dimensions.

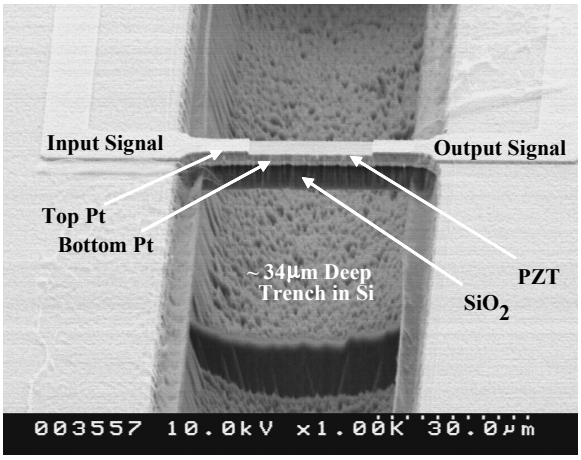


Figure 5. PZT MEMS Resonator for high frequency (GHz) filters applications.

## 4. Conclusion

A reactive ion etch process has been developed to reliably pattern up to 1 micrometer layer of low stress $SiO_2$PECVD film compatible for MEMS research applications. Some MEMS devices require achieving mechanical motion or vibration for its operation. In resonator devices the beam structures are designed and tuned to a very specific frequency for its intended application. The performance and functions of these devices depend on the material properties and precise pattern transfer of critical features. RIE of $SiO_2$ films play a vital role in the fabrication of MEMS devices. Micro fabrication methods have been developed at ARL to support research and fabrication of advanced electronic devices for MEMS applications.

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## Appendix A. Photo Resist Lithography Process

The following procedure describes the photolithography process:

1. Apply Clarion AZ5214 positive photo resist to achieve 1.7 microns film thickness.
   a) Spin speed 2000 rpm.
   b) Soft bake on hotplate at $120^0$C for 45 s.
   c) Expose mask on Karl-Suss MA-6 System.
   d) Exposure for 3.5 sec for total dose=70mJ/$cm^2$.
2. Develop in AZ 312 MIF solution for 60 s (dilution 1:1 ratio with DI water)
3. Rinse in DI water for 60 s.
4. Inspect for defects with aid of microscope.
5. Measure photo resist thickness using surface profilometer Tencor P-15 System.

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## Appendix B. Etching Parameters

**Lam 590 system etch parameters:**

| Parameter | Units |
|---|---|
| Pressure | 2.8 torr |
| $CF_4$ flow | 90 sccm |
| He flow | 170 sccm |
| $CHF_3$ flow | 30 sccm |
| Gap spacing | 1.35 cm |
| Time | Variable |
| Power | Variable |

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